AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A filter circuit, comprising:

~~in which~~ a plurality of unit circuits including a first stage unit circuit, at least one second stage unit circuit, and a final stage unit circuit ~~are~~ mutually connected in series, ~~computing means in~~ each of said unit circuits comprising a computing means;

said computing means in each of said first stage unit circuit and said at least one second stage unit circuit successively transmitting ~~transmits~~ to a unit circuit of a following stage unit circuit a computing result of a) an analog input signal sampled at a same sampling timing and b) a coefficient predetermined for each of said computing means,

said computing result of said computing means of each of said first stage unit circuit and said at least one second stage unit circuit being computed by

adding a value of a residual, from a previous stage unit circuit, and an analog computing result based on said analog input signal and a coefficient for said computing means, to obtain an added value,

low-bit quantizing said added value to obtain a quantization result,

subtracting a D/A converted value of the quantization result from the added value to obtain a residual value, and

successively transmitting said quantization result as said computing result and said residual value to a following circuit,

said computing means of each said first stage unit circuit and said at least one second stage unit circuit mutually adding ~~adds~~ said computing ~~results~~ result ~~of a present stage~~ and ~~it's a~~ computing result of an immediately preceding ~~previous~~ stage unit circuit so as to compute in ~~a~~ said final stage unit circuit ~~of a final stage~~ a cumulative value of computing results of all the coefficients and time-series analog sampling signals whose number corresponds to that of the coefficients, and the cumulative value is outputted as digital data,

wherein said previous stage residual and computing result values for said first stage unit circuit are default values

~~wherein low bit quantization is subjected to an added value of an output from a unit circuit of a previous stage and a computing result of the present stage, in an arbitrary unit circuit other than the final stage, and a quantization result and a residual, the residual being obtained by subtracting a D/A converted value of the quantization result from the added value, are successively transmitted to a following unit circuit~~.

2. (Currently Amended) A filter circuit, comprising:

~~in which~~ a plurality of unit circuits including a first stage unit circuit, at least one second stage unit circuit, and a final stage unit circuit ~~are~~ mutually connected in series, ~~computing means in~~ each of said unit circuits comprising a computing means;

said computing means in each of said first stage unit circuit and said at least one second stage unit circuit successively transmitting ~~transmits~~ to a unit circuit of a following stage unit circuit a computing result of a) an analog input signal sampled at a same sampling timing and b) a coefficient predetermined for each of said computing means,

said computing result of said computing means of each of said first stage unit circuit and said at least one second stage unit circuit being computed by

adding means for obtaining an added value,

low-bit quantizating said added value to obtain a quantization result,

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subtracting a D/A converted value of the quantization result from the added value to obtain a residual value, and

adding said quantization result to a cumulative value of a previous stage to produce said computing result,

said computing means of each said first stage unit circuit and said at least one second stage unit circuit mutually adding ~~adds~~ said computing ~~results~~ result ~~of a present stage~~ and ~~it's~~ a computing result of an immediately preceding ~~previous~~ stage unit circuit so as to compute in a said final stage unit circuit ~~of a final stage~~ a cumulative value of computing results of all the coefficients and time-series analog sampling signals whose number corresponds to that of the coefficients, and the cumulative value is outputted as digital data,

wherein the ~~computing result of the present stage is added to a cumulative value of a previous stage by adding means, the added value is subjected to low-bit quantization by an arbitrary unit circuit other than the final stage and is successively transmitted to a following unit circuit, a~~ D/A converted value of the ~~a~~ quantization result is subtracted from the added value so as to suppress an increase in a dynamic range of said adding means in a unit circuit of the following stage.

3. (Currently Amended) A filter circuit, comprising

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~~in which~~ a plurality of unit circuits including a first stage unit circuit, at least one second stage unit circuit, and a final stage unit circuit ~~are~~ mutually connected in series, ~~computing means in~~ each of said unit circuits comprising a computing means;

said computing means in each of said first stage unit circuit and said at least one second stage unit circuit successively transmitting ~~transmits~~ to a unit circuit of a following stage unit circuit a computing result of a) an analog input signal sampled at a same sampling timing and b) a coefficient predetermined for each of said computing means,

said computing result of said computing means of each of said first stage unit circuit and said at least one second stage unit circuit being computed by

adding means for obtaining an added value,

low-bit quantizating said added value to obtain a quantization result,

subtracting a D/A converted value of the quantization result from the added value to obtain a residual value, and

adding said quantization result to a cumulative value of a previous stage to produce said computing result,

said computing means of each of said first stage unit circuit and said at least one second stage unit circuit mutually adding ~~adds~~ said computing result ~~results of a present stage~~ and ~~its previous~~ a computing result of an immediately preceding stage unit circuit so as to compute in ~~a~~ said final stage unit circuit ~~of a final stage~~ a cumulative value of computing results of all the coefficients and time-series analog sampling signals whose number corresponds to that of the coefficients, and the cumulative value is outputted as digital data from said final stage unit circuit,

wherein said previous stage residual and computing result values for said first stage unit circuit are default values ~~low-bit quantization is subjected to an added value obtained by adding the computing result of the present stage to a cumulative value of a previous stage, a residual is computed by subtracting a D/A converted value of a quantization result from the added value so as to represent the cumulative value by a combined value of analog data and digital data, and at least the digital data is outputted from the unit circuit of the final stage~~.

4. (Currently Amended) A filter circuit, comprising:

~~in which~~ a plurality of unit circuits including a first stage unit circuit, at least one second stage unit circuit, and a final stage unit circuit ~~are~~ mutually connected in series, ~~computing means in~~ each of said unit circuits comprising a computing means;

said computing means in each of said first stage unit circuit and said at least one second stage unit circuit successively transmitting ~~transmits~~ to a unit circuit of a following stage unit circuit a computing result of a) an analog input signal sampled at a same sampling timing and b) a coefficient predetermined for each of said computing means,

said computing means of each said first stage unit circuit and said at least one second stage unit circuit mutually adding ~~adds~~ said computing result ~~results of a present stage~~ and ~~its previous~~ a computing result of an immediately preceding stage unit circuit so as to compute in ~~a~~ said final stage unit circuit ~~of a final stage~~ a cumulative value of computing results of all the coefficients and time-series analog sampling signals whose number corresponds to that of the coefficients, and the cumulative value is outputted as digital data,

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wherein said previous stage computing result value for said first stage unit circuit is a default value, comprising:

first adding means for mutually adding the computing result at the present stage and an output transmitted from a previous stage;

quantizing means which is provided in a unit circuit at the final stage and in a unit circuit at said at least one second stage unit circuit ~~an arbitrary~~

~~stage other than the final stage~~, and which performs low-bit quantization on an output from said first adding means;

second adding means for adding a quantization result, which is obtained by said quantizing means at the present stage, to a quantization result of the previous stage;

D/A converting means for performing analog conversion on an output from said quantizing means; and

third adding means which subtracts an output of said D/A converting means from an output of said first adding means, and which outputs a residual to a unit circuit of the following stage.

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5. (Currently Amended) A filter circuit, comprising:

~~in which~~ a plurality of unit circuits including a first stage unit circuit, at least one second stage unit circuit, and a final stage unit circuit ~~are~~ mutually connected in series, ~~computing means in~~ each of said unit circuits comprising a computing means;

said computing means in each of said first stage unit circuit and said at least one second stage unit circuit successively transmitting ~~transmits~~ to a unit circuit of a following stage unit circuit a computing result of a) an analog input signal sampled at a same sampling timing and b) a coefficient predetermined for each of said computing means,

said computing means of each said first stage unit circuit and said at least one second stage unit circuit mutually adding ~~adds~~ said computing result

~~results of a present stage~~ and a computing result of an immediately preceding ~~its previous~~ stage unit circuit so as to compute in ~~a~~ said final stage unit circuit ~~of a final stage~~ a cumulative value of computing results of all the coefficients and time-series analog sampling signals whose number corresponds to that of the coefficients, and the cumulative value is outputted as digital data wherein said previous stage values for said first stage unit circuit are default values, comprising:

first adding means for mutually adding the computing result at the present stage and an output transmitted from a previous stage;

quantizing means which is provided in a unit circuit at the final stage and in a unit circuit at said at least one second stage unit circuit ~~an arbitrary stage other than the final stage~~, and which performs low-bit quantization on an output from said first adding means;

second adding means for adding a quantization result, which is obtained by said quantizing means at the present stage, to a quantization result of the previous stage; and

D/A converting means which performs analog conversion on an output from said quantizing means, sends the output to the first adding means of the following stage, and subtracts the output from an output of said first adding means of the present stage.

6. (Original) The filter circuit as defined in claim 1, wherein

said arbitrary unit circuit is provided at every predetermined number of stages and a partial correlation value is periodically computed in accordance with said low-bit quantization.

7. (Original) The filter circuit as defined in claim 5, further comprising:

fourth adding means for subtracting an output of said A/D converting means of the final stage from an output of said first adding means of the final stage so as to obtain an analog residual thereof; and

A/D converting means with high resolution, that performs A/D conversion on an output from said fourth adding means.

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8. (Original) The filter circuit as defined in claim 5, further comprising:

first switching means which is provided between an analog input signal line and each of said computing means, and which inputs a reference voltage instead of the analog input signal;

second switching means for extracting a DC offset caused by inputting the reference voltage to each of the computing means during a calibration mode;

a memory for storing the DC offset; and

fifth adding means for subtracting the DC offset, which is stored in said memory, from a correlation output of said computing means at the final stage so as to correct the offset.

9. (Original) The filter circuit as defined in claim 5, wherein all second adding means are not equal in number of bits to the second adding means of the final stage, but the number of bits is gradually increased from a first stage to the final stage.

10. (Original) The filter circuit as defined in claim 5, wherein said quantizing means is a comparator, which performs binary or ternary quantization.

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11. (Original) The filter circuit as defined in claim 1, wherein the analog input signal is a spread spectrum receive signal, the coefficient is a spread code, each of said computing means is a correlation computing circuit for performing correlation computing on the spread spectrum receive signal and the spread code, said filter being a matched filter used for a spread spectrum receiver to perform reverse spread.

12. (Original) The filter circuit as defined in claim 11, wherein said computing means with M stages, which are an integral times larger than N number of code lengths of the spread code.

13. (Original) The filter circuit as defined in claim 11, wherein said computing means has M stages, which is equal to N code lengths of the spread code, respectively for an I component and a Q component, and an amplitude computing section is further provided.

14. (Original) The filter circuit as defined in claim 11, wherein K groups of said computing means with M stages are provided, said computing means at the same stage are equal in spread code, said respective computing means of each group receives clock signals, each having a phase shifted by 1/K of a chip period Tc, and

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a multiplexer is further provided for successively selecting and outputting a correlation output for every Tc/K from said computing means of the final stage in each of the groups.

15. (Original) The filter circuit as defined in claim 11, wherein said K computing means are connected in series at each of the M stages, and each of said computing means receives clock signals, each having a phase shifted by 1/K of a chip period Tc.

16. (Original) The filter circuit as defined in claim 11, wherein all the coefficients are set at "1" and an A/D converted value is computed regarding a moving average of an analog input signal.

17. (Original) The filter circuit as defined as claim 1, wherein some of the unit circuits connected in series are respectively provided in parallel into a plurality of columns, said computing means uses an analog input signal sampled at a similar sampling timing in the unit circuits of the stage that correspond with each other in the respective columns, and an added value of the coefficients of the corresponding stages is divided and set at a target coefficient value for the stage between parallel unit circuits.

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18. (Original) The filter circuit as defined in claim 17, wherein when a computing result of one of said columns is joined to the other column, a unit circuit of the other column has a) a multiplying coefficient of 0 regarding the analog input signal and b) a multiplying coefficient of 1, so that an analog residual of the one of the columns is inputted instead of the analog input signal and is added to an analog residual transmitted from a previous stage.

19. (Original) The filter circuit as defined in claim 17, wherein the analog input signal is a receive signal of a communication receiver or a signal subjected to frequency conversion, the coefficient determines a property of a band limitation filter, said each computing means is a correlation computing circuit for performing correlation computing on the receive signal of the communication receiver or the signal subjected to frequency conversion and the coefficient for determining a property of the band limitation filter, said filter

being a band limitation filter used for a converting section of a receive signal for a communication receiver.

20. (Currently Amended) A filter circuit having a plurality of correlation computing unit circuits for performing a predetermined computing on an analog input signal, which is subjected to sampling at a same timing, said computing unit circuits being connected in series so as to cumulate a partial correlation value ~~based on computing results~~,

wherein at least one of the correlation computing unit circuits except for a final stage, comprising:

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a first adder for adding ~~the~~ a computing result of said at least one correlation computing unit circuit and an output of a correlation computing unit circuit of a previous stage;

a quantization circuit for performing low-bit quantization on an output of said first adder;

a first delay circuit for delaying the computing result by a chip period;

a second delay circuit for delaying an output of said quantization circuit by a chip period;

a D/A converter for converting an output of said second delay circuit to an analog signal;

a second adder for adding a partial correlation value of the previous stage and an output of said quantization circuit;

a third delaying circuit for delaying an output of said second adder by a chip period so as to output as a partial correlation value to a correlation computing unit circuit of a following stage; and

a third adder for outputting a residual to the correlation computing unit circuit of the following stage, said residual being computed by subtracting an output of said D/A converter from an output of said first delay circuit.

21. (Original) The filter circuit as defined in claim 20, wherein among said correlation computing unit circuits, the correlation computing unit circuit for computing a partial correlation value by the low-bit quantization is determined according to resolution required for a correlation signal.

22. (Currently Amended) A filter circuit, comprising:

K (an integer) systems each having a plurality of correlation computing unit circuits, that perform a predetermined computing on an analog input signal producing a computing result in each computing unit circuit, which said analog input signal is subjected to sampling at a same timing, said correlation computing unit circuits being connected in series so as to cumulate a partial correlation value based on said computing result in each computing unit circuit ~~results~~, each said correlation computing unit circuit in a system of the K systems being a stage in the system,

wherein in said each system, at least one of said correlation computing unit circuits except for a final stage performs ~~low-bit quantization on an added~~

~~value~~ adding of the computing result computed in said at least one correlation computing unit circuit and an analog output of a correlation computing unit circuit of a previous stage to produce an added value, low-bit quantizing said added value to produce a quantization result, and the correlation computing unit circuit a) ~~adds~~ adding the quantization result and the partial correlation value of the previous stage and delays ~~an~~ said added value by a chip period so as to output an analog output ~~to be outputted~~ to the correlation computing unit circuit of a following stage, and b) delays the quantization result by a chip period to produce a delayed result, ~~and~~ D/A converting ~~a~~ said delayed result to produce a converted analog result, and ~~is subjected to D/A conversion so as to output~~ computing a residual ~~computed~~ by subtracting ~~a~~ said converted analog result from ~~the~~ said analog output based on said added value, said residual being ~~outputted to the~~ computed in the correlation computing unit circuit of a following stage,

the K systems operate in response to clock signals, each having a phase shifted by 1/K of a chip period, and

a selecting circuit is further provided for selecting a cumulated partial correlation value of each of the systems in response to the clock signal.

23. (Currently Amended) A filter circuit, comprising:

first and second systems having a plurality of correlation computing unit circuits, that perform predetermined computing on an analog input signal producing a computing result in each computing unit circuit, which said

analog input signal is subjected to sampling at a same timing, said correlation computing unit circuits being connected in series so as to cumulate a partial correlation value based on said computing result in each computing unit circuit ~~results~~, each said correlation computing unit circuit in a system of the first and second systems being a stage in the system,

wherein in said each system, at least one of said correlation computing unit circuits except for a final stage performs ~~low-bit quantization on an added value~~ adding of the computing result computed in said at least one correlation computing unit circuit and an analog output of a correlation computing unit circuit of a previous stage to produce an added value, low-bit quantizing said added value to produce a quantization result, and the correlation computing unit circuit ~~outputs~~ a) ~~adds~~ adding the quantization result and the partial correlation value of the previous stage and delays ~~an~~ said added value by a chip period so as to output an analog output ~~to be outputted~~ to the correlation computing unit circuit of a following stage, and b) delays the quantization result by a chip period to produce a delayed result, ~~and~~ D/A converting ~~a~~ said delayed result to produce a converted analog result, and ~~is subjected to D/A conversion so as to output~~ computing a residual ~~computed~~ by subtracting ~~a~~ said converted analog result from ~~the~~ said analog output based on said added value, said residual being ~~outputted to the~~ computed in the correlation computing unit circuit of a following stage,

said first and second systems operate in response to clock signals, each having a phase shifted by a half of a chip period, a common-mode component

of the analog input signal is inputted to said first system, an orthogonal component of the analog input signal is inputted to the second system, and an amplitude computing section is further provided for computing an amplitude value according to a cumulated partial correlation value of said first system and each cumulated partial correlation value of said second system and for outputting the amplitude value as an amplitude correlation output for every chip period.